11th International Conference



New Electrical and Electronic Technologies and their Industrial Implementation

Zakopane, Poland, June 25 – 28, 2019

Edited by Tomasz N. Kołtunowicz

ISBN: 978-83-7947-369-4

Publisher:Lublin University of Technology
20-618 Lublin, 38d Nadbystrzycka Str.Realization:Lublin University of Technology Library
e-mail: wydawca@pollub.pl

Error modeling in semiconductor memory of computers

P. Urbanovich 1,2

¹ Belarussian State Technological University, Minsk, Belarus ² Lublin Catholic University, Lublin, Poland, E-mail: pav.urb@yandex.by

Defects in semiconductor memory chips and errors of their functioning are of interest to both manufacturers of memory and their consumers [1]. Memory errors can be classified into soft errors, which randomly corrupt bits but do not leave physical damage; and hard errors, which corrupt bits in a repeatable manner because of a physical defect. Some time ago numerous studies concerning the distribution of failures and bit errors in chips and semiconductor memory systems were conducted (eg [2,3]).

Due to the increasing role of memory modules for the reliability of information systems in the last time, experts are turning more and more attention to this problem [4]. The research results led to a very important conclusion: memory errors are strongly correlated. This conclusion, in turn, allows to suggest that the distribution and interdependencies of defects over the area of memory chips, the time distribution of errors in telephone channels [5] and the distribution and types of errors in semiconductor memory systems have much in common. This means that in addition to the density of defects per unit area of a chip or the intensity of bit errors (the number per unit of time), the parameter of grouping (clustering) of defects and errors can be used for modeling of distribution of the bit errors in chips and in memory modules respectively.

The Poisson distribution and the Generalized Negative Binomial Distribution are used to simulate the distribution of defects both in individual chips and on whole semiconductor memory plates [1,2]. Such defects can be correlated with the corresponding types of bit errors in computer memory systems [4]. Based on these mathematical dependencies, it is possible to determine the degree of defects clustering in a chip. If we assume that defects in a chip (or its parts) with area ΔS are characterized by density *D* (per unit area), then the calculation of the average value of area (mathematical expectation) with *x* defects for the Poisson model can be calculated by the formula

$$\Delta S_x = \int_0^\infty \frac{1}{x!} (DS)^x \exp(-DS) dS \, .$$

Following the logic of reasoning, we can identify the parameter ΔS with time, t, and the parameter D – with the probability of occurrence of bit errors, p. On this basis, it is possible to model the distribution of bit errors with regard to their clustering [1].

References

- Urbanovich P.P., Alekseyev V.F., Vernikovskiy Ye.A.: Izbytochnost' v poluprovodnikovykh integral'nykh mikroskhemakh pamyati, Minsk: Navuka í tekhníka, 1995 (https://elib.belstu.by/ handle/123456789/24777)
- [2] Urbanovich P.P.: A model of defective memory cell distribution on LSI memory chips: Izvestiya vysshikh uchebnykh zavedenii. Radioelektronika, vol. 29 n.9, 1986, p. 92-95 (https://elib.belstu.by/handle/123456789/24780)
- [3] Vernikovskiy Ye.A., Urbanovich P.P.: Statisticheskiye kharakteristiki otkazov zapominayushchikh elementov v mikroskhemakh pamyati: Elektronnaya tekhnika. Ser. 3: Mikroelektronika, vol. 130 n.1, 1989, p.60-63 (https://elib.belstu.by/handle/123456789/25697)
- [4] B. Schroeder, E. Pinheiro, W.-D. Weber: DRAM Errors in the Wild: A Large-Scale Field Study/http://www.cs.toronto.edu/~bianca/papers/sigmetrics09.pdf
- [5] Urbanovich P.P., Patsey N.V., Spiridonov V.V.: Raspredeleniye oshibok v telefonnykh kanalakh peredachi diskretnoy informatsii: Izvestiya belorusskoy inzhenernoy akademii, vol 3 /No 1/, 1997, p.24-26 (https://elib.belstu.by/handle/123456789/26760)