OVERCOMING THE CHALLENGES OF THE QFN PACKAGE BY PROPER STENCIL GENERATION CHOICE (ELECTROFORM STENCILS, NANO-COAT STENCILS)

QFN – provides a ramification of benefits and reduced lead inductance, a small-sized "near chip-scale" footprint, skinny profile, and low weight. It further employment edge I/o cushions to ease the PCB following guiding. In addition, the uncovered copper die-pad innovation provides wonderful heat and electronic execution. These selections build the QFN associate optimum favorite for several new applications wherever size, weight, and thermal and electrical performance are essential.

Compared to other no-lead packages, they offer small form factor, good electrical and thermal performance, and are generally lower in cost. [1-3]. Manufacturers of high-reliability electronics systems, who rely on the commercial electronics supply chain for advanced packages, are showing increased interest in using FNS in their operations to meet miniaturization and functionality goals [4].

THE CHALLENGES OF QFNs

The signal pads ought to have a standoff height of two-three mils; If it deposits an excessive amount of solder within the center, the half will float up on the far side that height and forestall the signal contacts from to prevent this. We recommend smaller multiple openings within the stencil space for the middle pad - about fifty - eightieth glued coverage. As shown in Fig.1. we show the benefits of the windowpane apertures for the ground plane.



Figure. 1 Benefits of window pane apertures for the ground plane

2- the next challenge is the actual aperture size in the stencil. A reminder that any increase in the raised amount of solder in the center may still lead QFN to tilt to one side during re flow and pull out of the opposite side, leaving behind an open along the edge which produces in the lifting of the component.

Typical aperture widths as low as 0.175mm and aperture lengths as low as 0.4mm present a challenge to the printing process as far as percent paste transfer.

3- The solder masks One of the most crucial challenges associated with the quad flat-pack no-lead (QFN). We can divide the solder mask into three types:

1 - SMD, where the solder mask defines the pad opening on the board.

2- NSMD, where the pad itself defines the boundary of the pad and the solder mask, is pulled back off the pad (typically 0.05 to 0.075mm per side).

3- NSMD – Window. In the third case, there are no solder masks among pads, accordingly bridging among pads is a lot of than with solder mask among pads.



Figure 2. Solder Mask Designs

Design Considerations for Stencil and PCB

We notice in the Table.1 stencil design for the three solder mask cases as shown in table1 below.

In the case NSMD, the stencil aperture is 1-1 with the PCB pad dimension. We note that the suggested length of the pad on the PCB compared to the length of the lead on the QFN is 0.2 mm larger.

As shown, the area ratio for a 0.125mm thick stencil is >0.66 for all the examples listed.

- The aperture size for the SMD is 0.05 mm smaller than the PCB pad.

| Package | PitchI/O | Package Lead Width | Package Lead Length | PCB PCB | Aperture NSMD | Aperture NSMD | Stencil Thickness | Area Ratio |
|---------|----------|--------------------------|---------------------------|------------|------------------|------------------|----------------------|---------------|
| 3mm | .5mm 12 | .23mm | .55mm | .23mm.75mm | .23mm | .75mm | .125mm | 0.70 |
| 4mm | .5mm 20 | .25mm | .40mm | .25mm.60mm | .25mm | .60mm | .125mm | 0.71 |
| 7mm | .5mm 44 | .25mm | .55mm | .25mm.75mm | .25mm | .75mm | .125mm | 0.75 |
| 10mm | .5mm 72 | .23mm | .40mm | .25mm.60mm | .25mm | .60mm | .125mm | 0.71 |
| 12mm | .5mm 80 | .25mm | .55mm | .25mm.75mm | .25mm | .75mm | .125mm | 0.75 |

- If the stencil is misaligned to the PCB, the paste could print if the

stencil is misaligned to the PCB on the solder mask.

- Maybe there are high-stress points if the solder contacts the mask. The reduction in aperture size has reduced the realm magnitude relation, creating paste transfer harder.

- For Area (.66), Nano-coated is stenciling suggest.

The last NSMD–Window. The pitch is (4mm), exploit very little space to place a solder mask between pads on the PCB. Aperture size is also a small giving a challenging Area Ratio of (.125mm) thick stencils; therefore .100mm We normally recommend thick stencils to provide a more robust stencil printing process window.

Stencil Design for Typical QFN Apertures (NSMD)

Stencil Design for Typical QFN Apertures (SMD)

| Package | PitchI/O | Package Lead Width | Package Lead Length | PCB P | CB ² | Aperture SMD | Aperture SMD | Stencil Thickness | Area Ratio |
|---------|----------|--------------------------|---------------------------|----------|-----------------|-----------------|-----------------|----------------------|---------------|
| 3mm | .5mm 12 | .23mm | .55mm | .23mm.75 | mm | .18mm | .70mm | .125mm | 0.57 |
| 4mm | .5mm 20 | .25mm | .40mm | .25mm.60 |)mm | .20mm | .55mm | .125mm | 0.59 |
| 7mm | .5mm 44 | .25mm | .55mm | .25mm.75 | Smm | .20mm | .70mm | .125mm | 0.62 |
| 10mm | .5mm 72 | .23mm | .40mm | .25mm.60 |)mm | .18mm | .55mm | .125mm | 0.54 |
| 12mm | .5mm 80 | .25mm | .55mm | .25mm.75 | mm | .20mm | .70mm | .125mm | 0.62 |

Stencil Design for Typical QFN Apertures (NSMD window)

| Package | Pitch | I/O | Package | Package | PCB | PCB | Aperture | Aperture | Stencil | Area |
|---------|-------|-----|---------|---------|--------|--------|----------|----------|-----------|-------|
| _ | | | Lead | Lead | | | SMD | SMD | Thickness | Ratio |
| | | | Width | Length | | | | | | |
| 4mm | .4mm | 32 | .175mm | .45mm | .175mm | .610mm | .175mm | .560mm | .125mm | 0.53 |
| | | | | | | | | | | |
| 4mm | .4mm | 32 | .175mm | .45mm | .175mm | .610mm | .175mm | .560mm | .100mm | 0.67 |
| | | | | | | | | | | |

Expected problems and proposed solutions

- hassle arises once the employment of an NSMD window while the solder masks are beyond the pad on the PCB. During this design, it extrudes the solder paste via the stencil for the explanation that the stencil isn't in grips with the PCB pads at some stage in printing. This extruded paste can bite the very cheap side of the stencil, inflicting ability bridging at some stage in consecutive prints insight that there are no solder masks between neighboring pads. Stencil wiping when every print could, also, assist scale back this problem. An Example of an NSMD — Window PCB with solder mask above the height of the PCB pads.

- A solution offered could be a PCB facet step stencil, as shown in Figure.5. it's Associate in Electroform stencil, which is (.08mm) thick everyplace except within the QFN space within the solder mask where it's (.01mm) thick. Here the mask gap was of the order of (.125mm) per facet except on the ends of the pad rows wherever it had been less.

- There are many limitations to the present approach. especially, the spacing between the step and therefore the solder mask is minimum, allowing very little misregistration. Also, the stencil is an agent for all alternative elements except the QFN, which can yield deficient paste.

- may address the primary limitation at the PCB style level by creating the mask to pad clearance abundant larger; of the order of(.25mm) per facet and departure the bottom plane with no solder mask close.

- The second proposal to resolve the matter could be a single level stencil whereas not a step with Nano-Coating on the aperture walls and on lowest (PCB side) of the stencil. the Nano-Coatings should have a property called fluxophobicity. The stencil will stop the flow of flux on its surface. it's live sort of the 'Flux Contact Angle. this can be the angle that the flux can type once a drop is placed on the surface of the stencil.

- The reason for selecting Nano-coating not entirely can increase the paste ability to unhitch from the apertures conjointly to resist spreading on the terribly second aspect of the stencil once the paste creates into a cavity shaped by the NSMD- Window.

- This property not entirely eliminates the need for frequent belowboard wiping; but, it to boot reduces the incidence for a pad to pad bridging.

ALGORITHM OF QFN Repair

The algorithm of the repairing of a defective QFN device presented in Fig.3



Fig. 3. Algorithm design methods PCB

Conclusion

Although QFN devices gift a venture to the SMT assembly system with right stencil design, proper stencil generation choice (Laser stencils, Electroform stencils, Nano-Coat stencils), and adequate PCB solder mask layout those demanding situations may be overcome.

REFERENCES

1] Li Li, "Reliability Modelling and Testing of Advanced QFN Packages", proceedings of 2013 ECTC conference, pp. 725-730.

[2] Ahmer Syed and WonJoon Kang, "Board Level Assembly and Reliability Considerations for QFN Type Packages", proceedings of 2003 SMTA conference, USA.

[3] Guofeng Xia, Fei Qin, Wenhui Zhu et al. "Comparative Analysis of Reliability Between Dual-row and Conventional QFN Packages", proceedings of 2012 Int. Conf. on Electronic Packaging Technology & High Density Packaging, pp. 616-618.